## REMARKS

This Amendment is in response to the Office Action dated October 4, 2004. In the Office Action, the Examiner rejected claims 1-22 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 7, 15 and 17 are amended, as shown above, to more clearly recite features of the claimed invention. Claim 17 has been amended to correct its dependency to claim 15. Claims 1-22 remain pending in the application. For the reasons set forth below, the Applicants respectfully request reconsideration and allowance of all pending claims.

Acknowledgement of Preliminary Amendment

The applicants request the Examiner acknowledge receipt and entry of the preliminary amendment mailed March 27, 2001. In this preliminary amendment, amendments were made to claims 2, 3, and 4. The amendments were correctly shown in the "Version of Amended Claims with Markings" section. However, in the "clean" version, the original claims were inadvertently recited instead of the amended version of claims 2, 3, and 4. The applicants respectfully request that the version of claim 2, 3, and 4 listed in the "Version of Amended Claims with Markings" section be entered.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

With respect to the rejection of claims 1-22, the Examiner has identified claim language in independent claims 1, 7, and 15 that is inconsistent with the specification. The applicants acknowledge that the language in the originally-filed claims 1 and 7 was in error, and thanks the Examiner for pointing out the inconsistencies. Claims 1 and 7 have been amended to correct these inconsistencies in view of the Examiner's comments.

With respect to the comment that claim 7, line 15, "said message data" lacks antecedent basis, the applicants respectfully direct the Examiner's attention to line 13 of claim 7, which recites

... bus that enables a transfer of message data from .... Accordingly, there is proper antecedent basis for "said message data" in line 15.

With respect to claim 15, this claim has been amended to correct for an inadvertent error. With further regards to claim 15, the Examiner states,

> Regarding claim 15, the language of the claim refers to figure 5, however, it seems that the three steps, for lines 10-16, are not a part of figure 5. It is unclear what is intended to be the claimed limitation by reciting those three steps.

Applicants respectfully assert that the three operations defined by lines 10-16 are part of the MAC Bus Out connection depicted in Figure 5, (as well as Figures 9 and 10). With further regards to the language used in claim 15, the specification recites:

> The handshake signal definitions used in both the MAC Bus In and Out interfaces are identical, so it is also appropriate to speak of the sending side and the receiving side of the interface. The sending side always initiates data packet transfers by asserting data and a corresponding transfer request signal. The receiving side controls the actual transfers by asserting its xfr (transfer) signal during cycles when it latches data from the sending side. (Page 9, lines 10-16);
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> The MAC Bus Out connection supports data flow from System side blocks to the Network side blocks. As the Network must determine the general timing and order of transfers, the MAC Bus Out interface must include both a *forward data transfer interface* and a *reverse request message interface* by which the network side can indicate the order and size of data transfers it requires. The reverse request message interface is similar to the forward data transfer interfaces of the In and Out connections except that it is limited to one word transfers. Those words correspond closely with the packet header words of the data transfer interfaces. (Page 10, lines 9-18);
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> The set of MAC Bus Out interface communication signals corresponding to sending data from the System side to the Network side is shown in FIGURE 5. As discussed above, sending data out requires the Network side to determine the general timing and order of transfers. Accordingly, the Mac Bus Out interface includes a forward data transfer interface 39 comprising a **request** signal 40, a **hold** signal 42, a **xfr** signal 44, and **data** 46, as well as a reverse request message interface 41

comprising an **mrequest** signal 48, an **mxfr** signal 50, and an **mdata** message word 52. A data transfer out operation is initiated by the System side by asserting **request** signal 40 and **data** 42. The Network side then controls transfer of **data** 42 by asserting **xfr** signal 44. In a manner similar to MAC Bus In interface 31, **hold** signal 42 may be asserted by the System side during a cycle to indicate that the System side will not be able to update **data** 46 at the end of the current cycle, introducing a wait state on the next cycle if the System side performs a **xfr** signal 44 while **hold** signal 42 is asserted. (Page 14, line 18 – Page 15, line 11); and

Further communications control is enabled through the data request messages passed from the Network side to the System side over reverse request message interface 41. These messages are passed in a manner substantially similar to that discussed above with respect to the MAC Bus In interface 31, except that the message data is moving in the opposite direction, and is limited to one word transfers (there is no equivalent to hold signal 38), wherein **mrequest** 48 is asserted to request transfer of a request message from the Network side while asserting a **mdata** message word 52 and **mxfr** signal 50 is asserted to indicate that the System side is latching **mdata** message word 52 at the end of the current cycle. (Page 15, lines 12-22)

Thus, the operations of lines 10-16 relate to the reverse request message interface depicted in Figure 5, which includes transfer message data (mdata message word 52) ("sending transfer message data from the receiving side block to the sending side block'), a transfer message data request (mrequest) signal 48 ("asserting a transfer message data request signal from the receiving side block to the sending side block"), and a transfer message data transfer signal (mxfr) signal 50 ("issuing a transfer message data transfer signal from the sending side block to the receiving side block to inform the receiving side block that the sending side block is latching the transfer message data". Accordingly, it is respectfully asserted that the invention recited in claim 15 is supported by language and drawings provided in the specification of the present application.

The Examiner states, "Claims 1, 7 and 15 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action." Applicants respectfully assert that each of independent claims 1, and 7 have been appropriately amended to meet the requirements of 35

U.S.C. § 112, and that claim 15, as originally presented (absent the minor correction to line 10), recited an invention that met the requirements of 35 U.S.C. § 112. Accordingly, each of independent claims 1, 7, and 15 are now in condition for allowance. Additionally, the dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

*Charge Deposit Account*

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

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